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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,812	03/22/2004	Raul Alejandro Perez	TI-36957	1062

23494 7590 03/24/2006

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,812	PEREZ, RAUL ALEJANDRO	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 2/21/06.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 9 and 15 is/are allowed.

6)☒ Claim(s) 1-8,10-14 and 16-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/21/06 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 is indefinite because it is unclear what current loop that the cited "error amplifier" belongs.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 3, 4, 6, 7, 10, 11, 19 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsuchiya (USP 6812781).

As to claim 1, Tsuchiya's figure 1 shows a method of stabilizing two current loops within a circuit comprising the steps of: providing a main current loop (30) utilizing negative feedback for supplying current to a load: providing a sensing loop (10) utilizing negative feedback for controlling the current to the load; an error amplifier (30) for the main current loop coupled to the output of an error amplifier for the sensing loop such that the capacitance of each loop is isolated from that of the other loop; and providing a compensating capacitor (C1 and C2 in figure 2) to each loop whereby stability is independently maintained for each loop within selected operational criteria.

As to claim 3, figure 2 shows that the output of the main loop error amplifier comprises a first node having a higher impedance than a second node (gate of 52), the compensating capacitor being coupled to the second node.

As to claim 4, figure 2 shows that the output of the main loop error amplifier comprises a first node having a higher impedance than a second node (gate of 52), the compensating capacitor being coupled to the first node (via R2).

As to claim 6, figure 2 shows a circuit having a low capacitive load and comprising two stable current loop sub circuits further comprising: a main current loop (30) for supplying current to the load, the main current loop having a negative feed back loop utilizing a first compensation capacitor (C2) for maintaining stabilizing within a pre-selected operational range, a sensing loop (10 for controlling the current to the load, the sensing loop having a negative feedback loop utilizing a second compensation capacitor for maintaining stabilizing within a pre-selected

operational range; and a transistor (52) for coupling the output of the main current loop error amplifier (32-40) and the output of the sensing loop such that the first compensation capacitor is isolated from the second compensation capacitor.

As to claim 7, figure 2 shows that the transistor further comprises a MOSFET.

As to claim 10, figure 2 shows that the main loop further comprises a main load error amplifier having a plurality of output nodes (source of 38 and drain of 32) wherein the output of the main loop error amplifier comprises a lower impedance node of the error amplifier.

As to claim 11, figure 2 shows that the main loop error amplifier further comprises an error amplifier having a plurality of output nodes (drain of 52 and gate of 52) and wherein the output of the main loop comprises a higher impedance node of the error amplifier.

As to claims 19 and 20, figure 2 shows that the sensing loop limits the maximum current to the load.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5, 12, 13, 14 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchiya (USP 6812781).

As to claims 5 and 12, Tsuchiya fails to teach that the main loop comprises low dropout (LDO) voltage regulator. However, it is notoriously well known in the art that LDO voltage regulator proving stable supply voltage. Therefore, it would have been obvious to one having

ordinary skill in the art to use LDO voltage regulator as a supply circuit for supplying VDD to the main loop for the purpose of operating the circuit figure 1 precisely.

As to claims 13, 14, 16 and 17, Tsuchiya's figure 2 shows all limitations of the claims except for 1 μF capacitance. However, it is well known in the art that the size of the capacitor determines how smooth the output going to be. It is seen as an obvious design preference to select particular value for the load capacitor dependent upon particular environment of use to ensure optimum performance. Therefore, it would have been obvious to one having ordinary skill in the art to use 1μF capacitor for figure 2 capacitors the purpose of reducing output noise.

As to claim 18, it is seen as an intended use for using the circuit in a LDO voltage regulator.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchiya (USP 6812781) in view of Cartwright (USP 4064506).

Tsuchiya's figure 2 fails to show that the transistor is bipolar transistor. However, Cartwright teaches in col. 5, lines 35-47, that bipolar transistors have an advantage over FET's in that their transconductances tend to be little affected by emitter-to-collector potential variations. Therefore, it would have been obvious to one having ordinary skill in the art to replace Tsuchiya's transistors with bipolar transistors for the purpose of improving the circuit performance.

Allowable Subject Matter

9. Claims 9 and 15 are allowed.

10. Claim 2 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim 2 would be and claims 9 and 15 are allowable because the prior art fails to teach or suggest that the output of the error amplifier of the main current loop coupled to the gate of a transistor and the compensating capacitor of the sensing loop coupled to the source of the transistor.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

March 21, 2006